Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1.(original) A data regenerator for regenerating a data signal, comprising:

a convertor for converting a received data signal into a binary data signal in dependence on conversion parameters;

an error corrector for correcting errors in the binary data signal based on error correction code contained in the binary data signal to produce a corrected binary data signal; and

a performance monitor for comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and logic "0"s that have been corrected by the error corrector and output a feedback signal representative of said information;

wherein the convertor adjusts at least some of the conversion parameters in dependance on the feedback signal.

2. (original) The data regenerator of claim 1 wherein the adjusted conversion parameters include a slicing level for the received data signal to distinguish between a logic "1" and a logic "0".

3. (original) The data regenerator of claim 2 wherein the adjusted conversion parameters include a sampling phase.

4. (original) The data regenerator of claim 2 wherein the received data signal is an optical data signal transmitted over a fiber path and the converter includes an opto/electrical transducer for converting the received data signal into an electrical data signal.

5. (original) The data regenerator of claim 4 wherein the converter includes an analog to digital convertor for sampling an analog electrical signal output from

the opto/electrical transducer in dependence on the slicing level to produce the binary data signal.

6. (original) The data regenerator of claim 5 wherein the analog to digital convertor has a sampling phase that is adjusted in dependence on the feedback signal.

7. (original) The data regenerator of claim 1 wherein the adjusted conversion parameters are adjusted with respect to achieving a threshold balance in the ratio of corrected logic "1"s and "0"s.

8. (original) The data regenerator of claim 1 wherein the performance monitor includes:

a comparitor for performing a bitwise comparison of the corrected binary data signal and the uncorrected representation of the binary data signal and generating a first signal when the comparitor detects that a logic "1" has been changed to a logic "0" and a second signal when the comparitor detects that a logic "0" has been changed to a logic "1" by the error corrector; and

a duty cycle generator responsive to the first and second signals for generating the feedback signal, the feedback signal being indicative of the ratio of corrected logic "1"s to corrected logic "0"s for predetermined durations of the data signal.

9. (original) The data regenerator of claim 8 including a descrambler for descrambling the binary data signal output by the convertor to produce an uncorrected binary data signal that is provided to the error corrector, the performance monitor including rescrambling means for rescrambling the uncorrected binary data signal and the corrected binary data signal, the comparator performing the bitwise comparison on the rescrambled data signals.

10. (original) The data regenerated of claim 1 wherein the performance monitor includes counting means for counting a number of logic "1"s and a number of logic "0's that have been corrected by the error corrector for a predetermined

duration of the binary data signal, and outputting signals representative of the number of corrected logic "1"s and corrected logic "0"s.

11. (original) A method for regenerating a binary data signal comprising:

converting a received data signal into a binary data signal according to conversion parameters;

detecting and correcting errors in the binary data signal based on detection and correction code included in the binary data signal to produce a corrected binary data signal;

comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and "0"s that have been corrected; and

adjusting at least one of the conversion parameters in dependence on the determined information.

12. (original) The method of claim 11 wherein the received data signal is an optical data signal, including converting the optical data signal into an analog electrical signal and sampling the analog electrical signal in accordance with a sampling phase to determine, relative to a threshold slicing level, if the samples represent logic "1"s or logic "0"s, to produce the binary data signal.

13. (original) The method of claim 12 including adjusting the threshold slicing level in dependence on the determined information.

14. (original) The method of claim 13 including adjusting the sampling phase in dependence on the determined information.

15. (original) The method of claim 11 wherein the conversion parameters are adjusted with respect achieving a threshold balance in the ratio of corrected logic "1"s and "0"s.

16. (original) The method of claim 11 wherein the received data signal includes a plurality of data frames formatted as Optical Transport Units, including a

generating a duty cycle wave-form having successive periods, each period being representative of the ratio of corrected logic "1"s and "0"s in at least one of the data frames.

17. (original) A performance monitoring device for monitoring the performance of a data regenerator that corrects a received data signal based on forward error correction information contained in the received data signal, comprising:
comparison means for receiving a corrected binary data signal and an uncorrected binary data signal from the data regenerator and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals to determine when a logic "1" has been corrected to a logic "0" and when a logic "0" has been corrected to a logic "1" by the data regenerator; and
signal generating means responsive to the comparison means for generating an output representative of the relative number of corrected logic "1"s and logic "0"s.

18. (original) The performance monitoring means of claim 17 wherein the signal generating means generates a duty-cycle waveform representative of the ratio of corrected logic "1"s and logic "0"s for a data signal of a predetermined length.

19. (original) The performance monitoring means of claim 18 wherein the performance monitoring device includes rescrambler means for rescrambling an unscrambled corrected binary data signal and for rescrambling an unscrambled uncorrected binary data signal and providing the rescrambled signals to the comparison means for said bit-by-bit comparison.

20. (original) The performance monitoring means of claim 17 wherein the signal generating means includes means for counting a number of corrected logic "1"s and a number of corrected logic "0"s for a data signal of a predetermined length, and outputting signals representative of said number of corrected logic "1"s and said number of corrected logic "0"s.